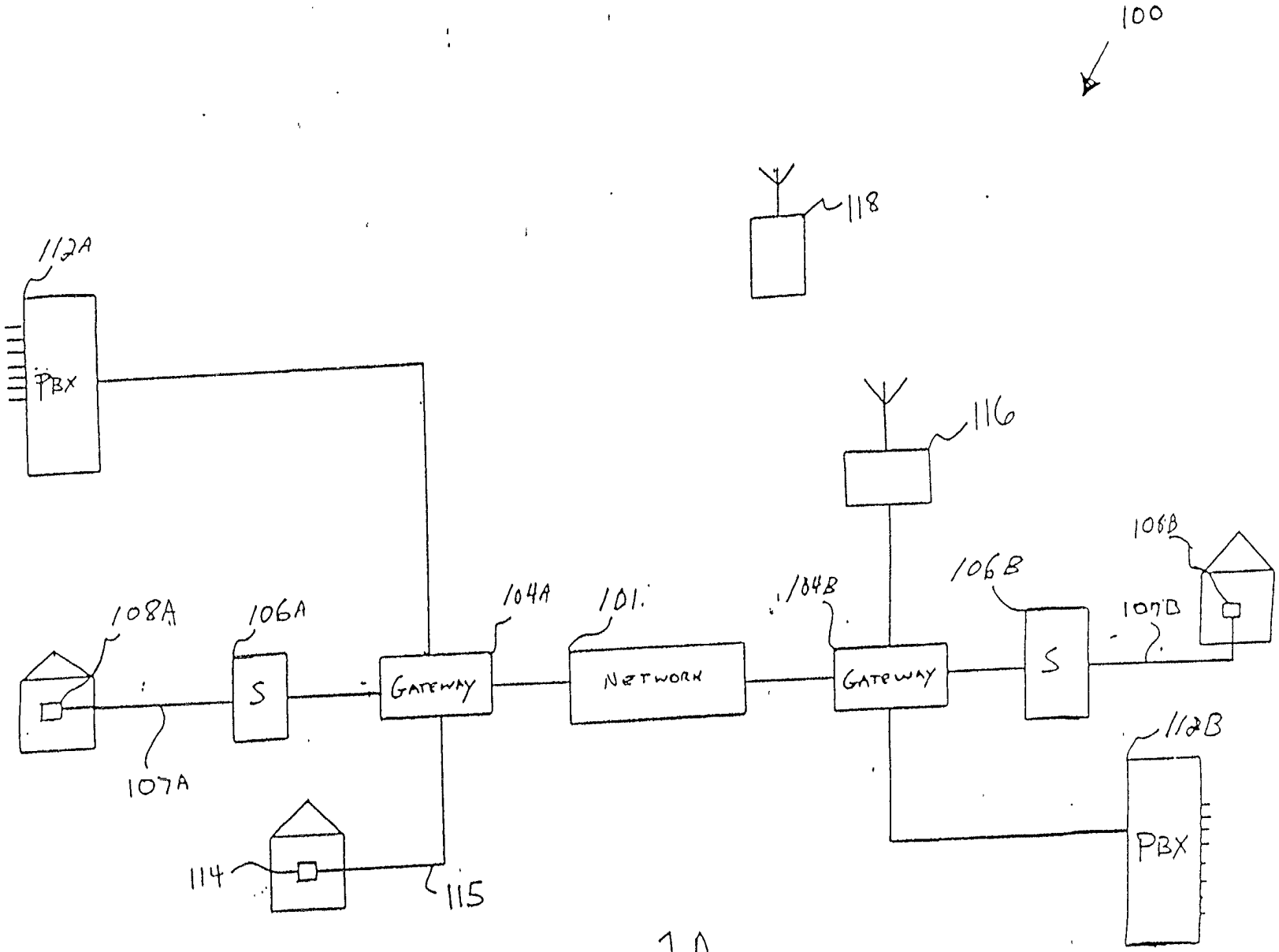

100
118
112A
PBX
116
108A
106A
104A
101
104B
106B
106B
107B
S
GATEWAY
NETWORK
GATEWAY
S
107A
112B
114
115
PBX

FIG. 1A

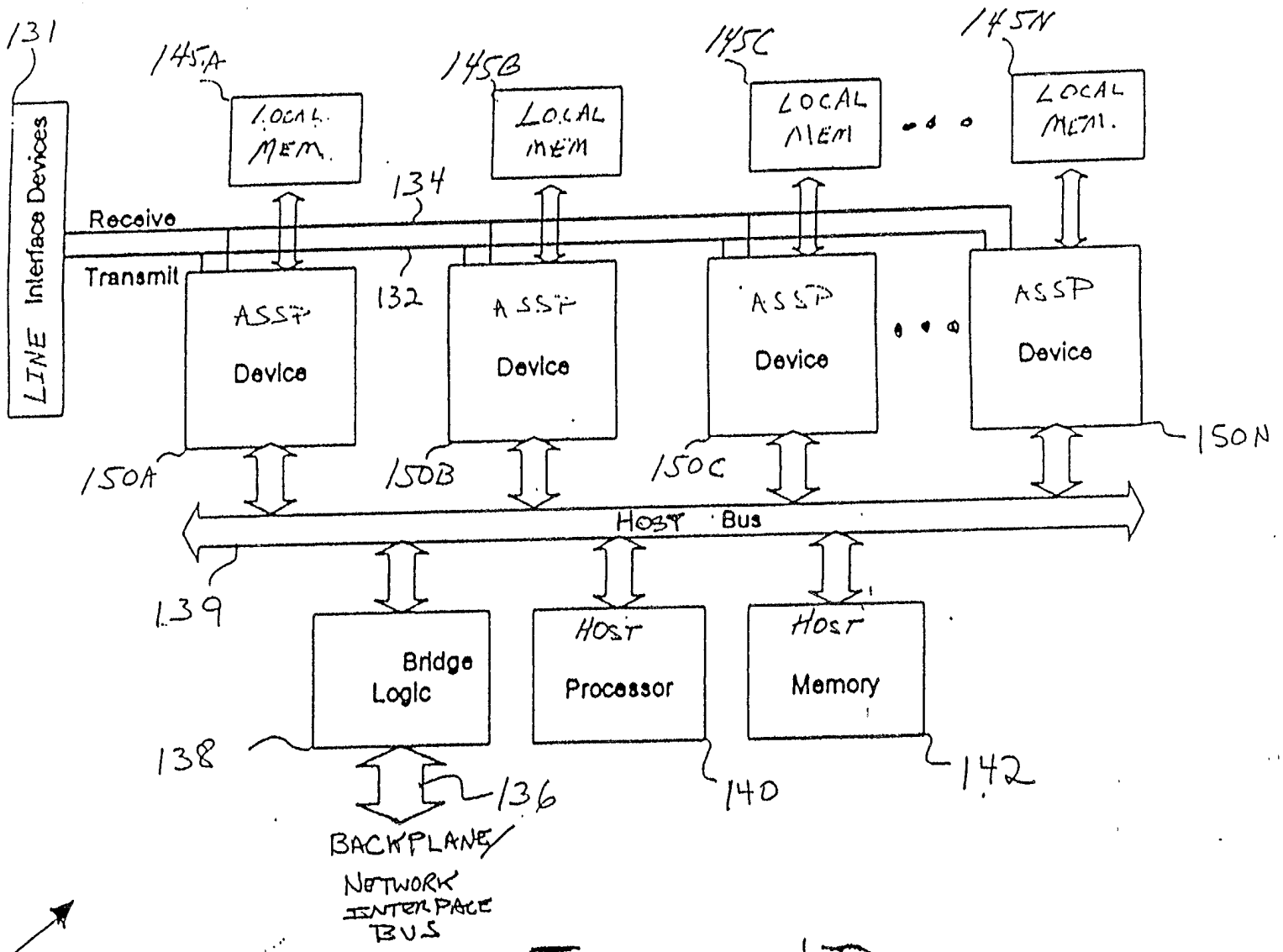

131
LINE Interface Devices
145A
LOCAL MEM.
145B
LOCAL MEM
145C
LOCAL MEM
145N
LOCAL MEM.
134
Receive
Transmit
132
ASSP Device
ASSP Device
ASSP Device
ASSP Device
150A
150B
150C
150N
Host Bus
139
Bridge Logic
Host Processor
Host Memory
138
136
140
142
BACKPLANE
NETWORK INTERFACE BUS
130

FIG. 1B

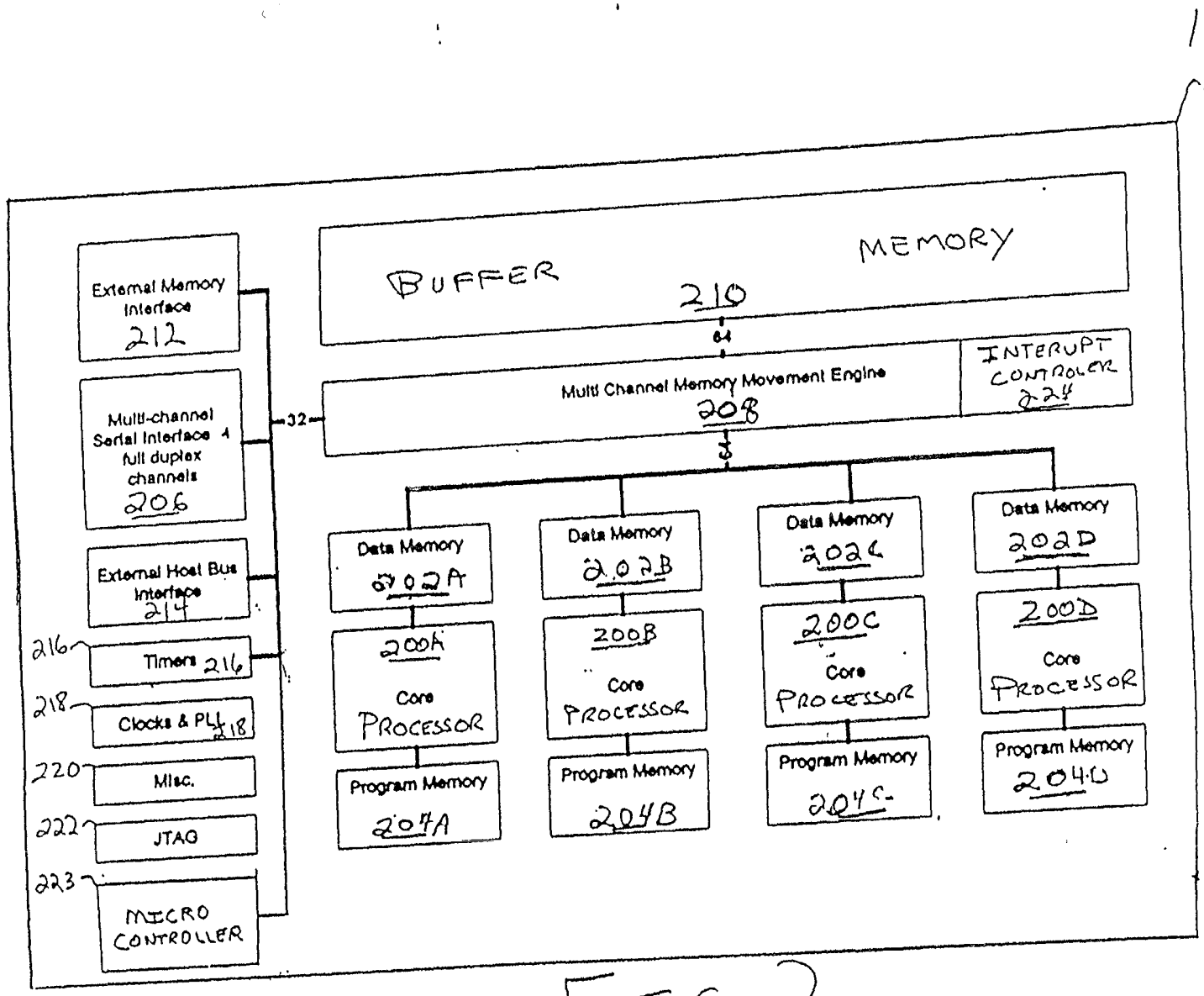

150
BUFFER MEMORY
210
External Memory Interface 212
Multi-channel Serial Interface 4 full duplex channels 206
External Host Bus Interface 214
Timers 216
Clocks & PLL 218
Misc. 220
JTAG 222
MICRO CONTROLLER 223
32
Multi Channel Memory Movement Engine 208
INTERUPT CONTROLLER 224
64
Data Memory 202A
Data Memory 202B
Data Memory 202C
Data Memory 202D
200A Core PROCESSOR
200B Core PROCESSOR
200C Core PROCESSOR
200D Core PROCESSOR
Program Memory 207A
Program Memory 204B
Program Memory 204C
Program Memory 204D

FIG. 2

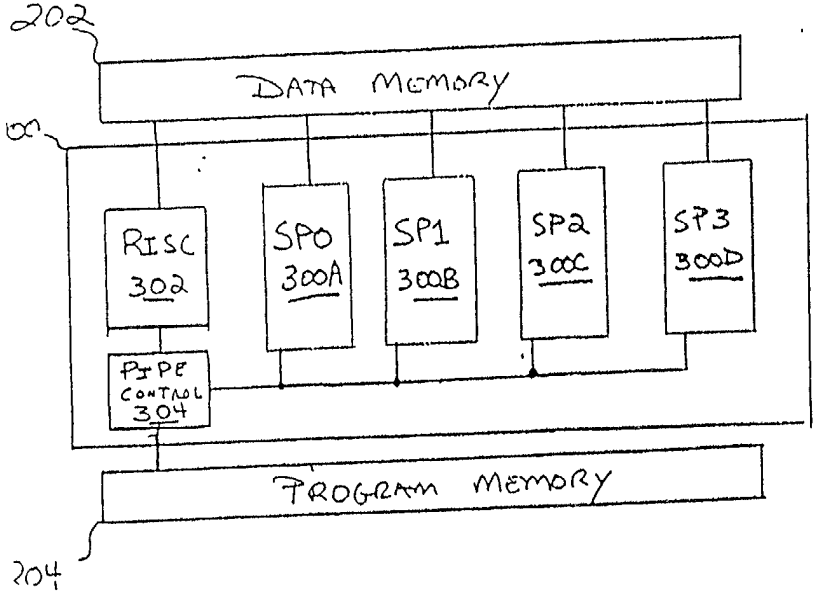


FIG. 3

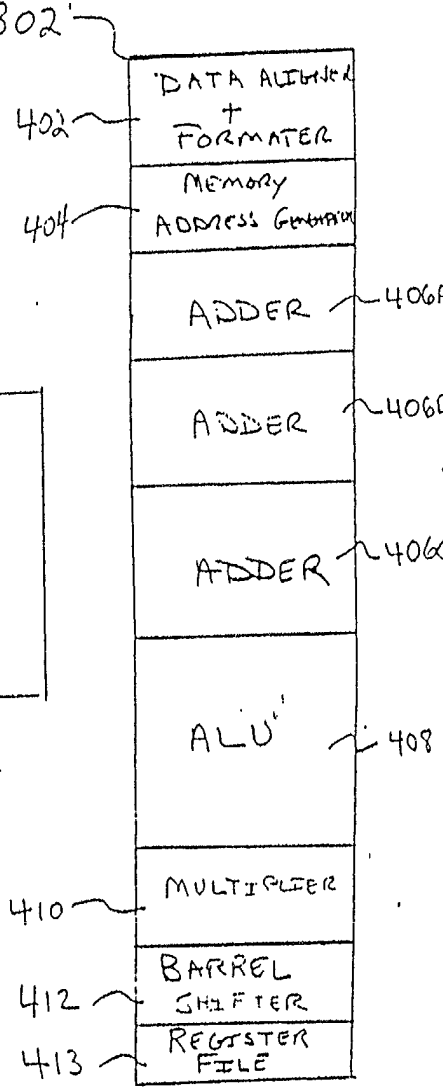


FIG. 4

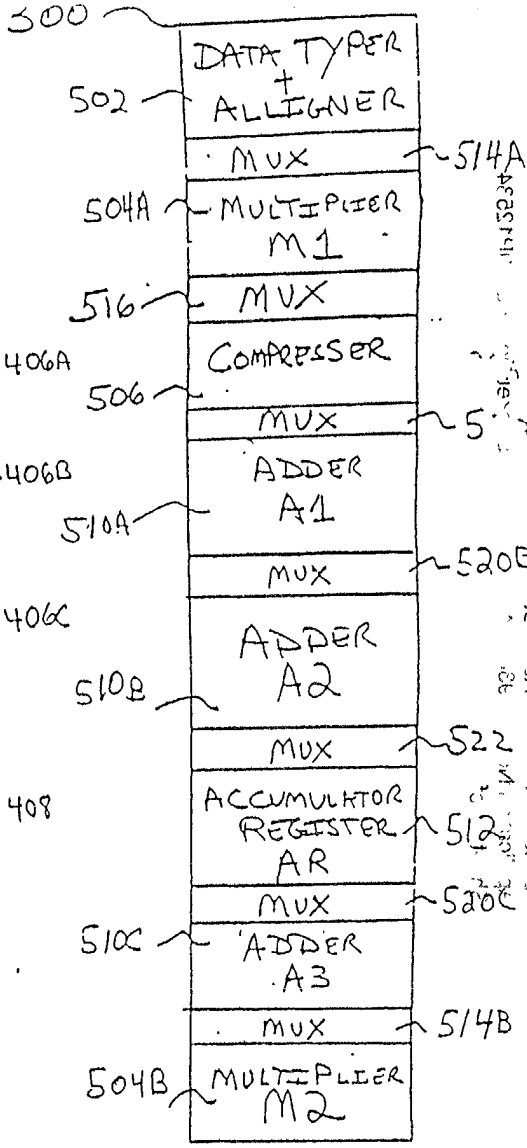


FIG. 5A

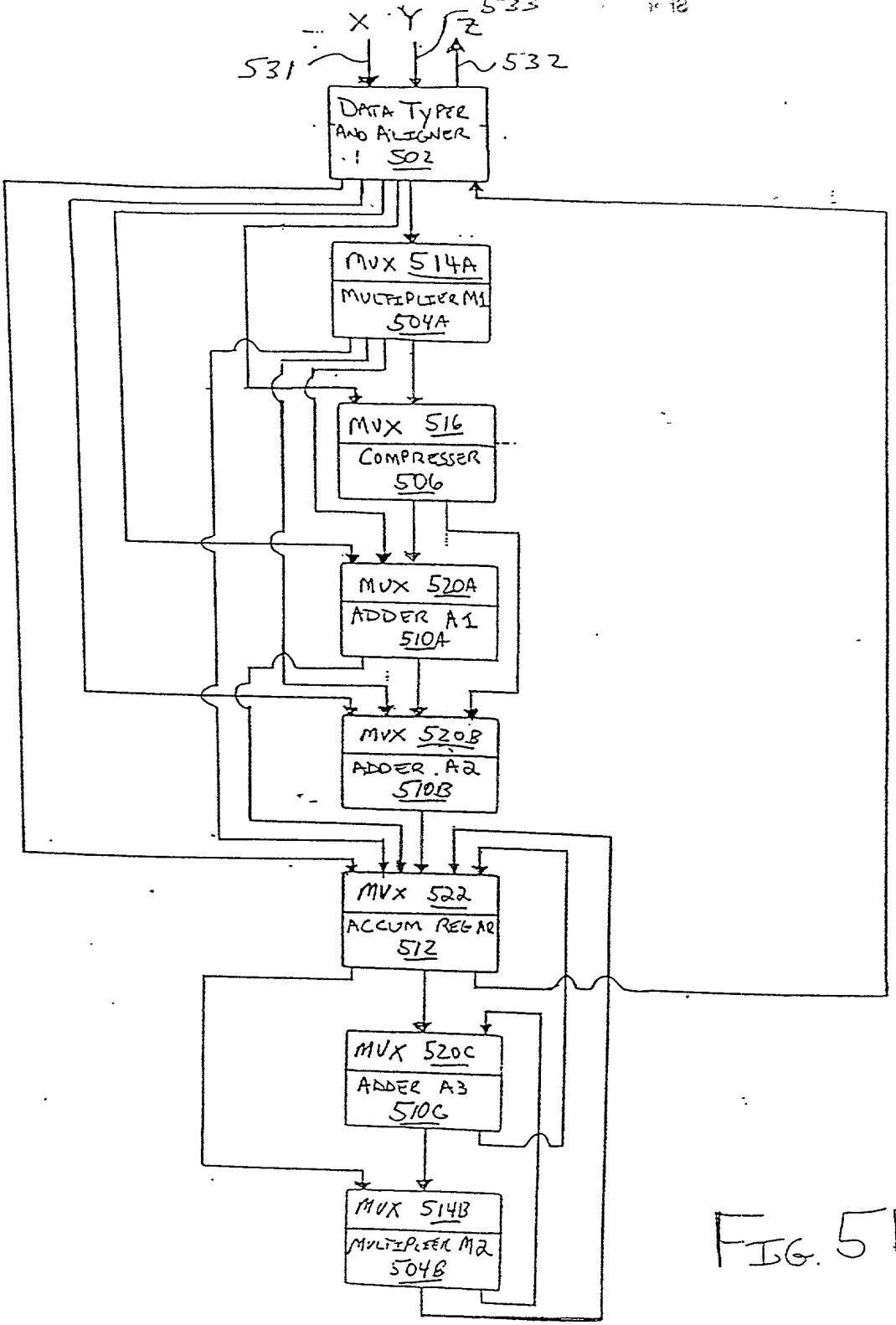

X
Y
Z
533
531
532
DATA TYPER AND ALIGNER 502
MUX 514A
MULTIPLIER M1 504A
MUX 516
COMPRESSER 506
MUX 520A
ADDER A1 510A
MUX 520B
ADDER A2 510B
MUX 522
ACCUM REGAR 512
MUX 520C
ADDER A3 510C
MUX 514B
MULTIPLIER M2 504B

FIG. 5B

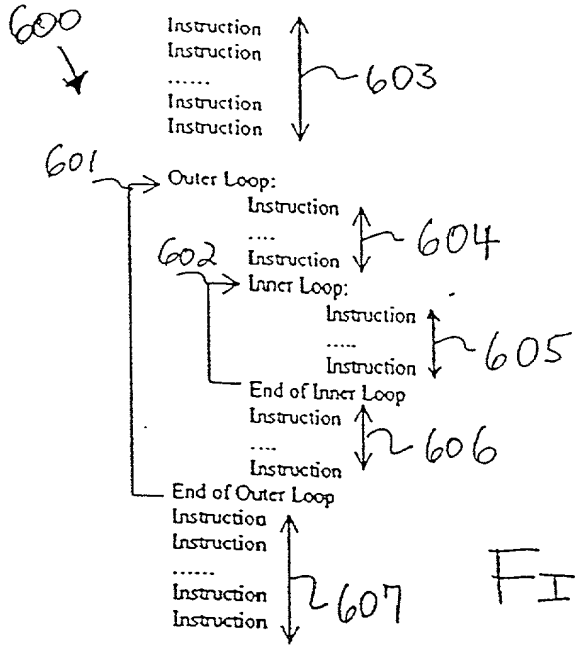


FIG. 6A

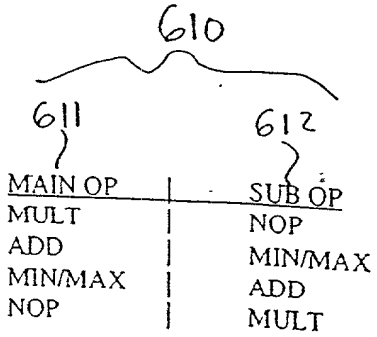


FIG. 6B

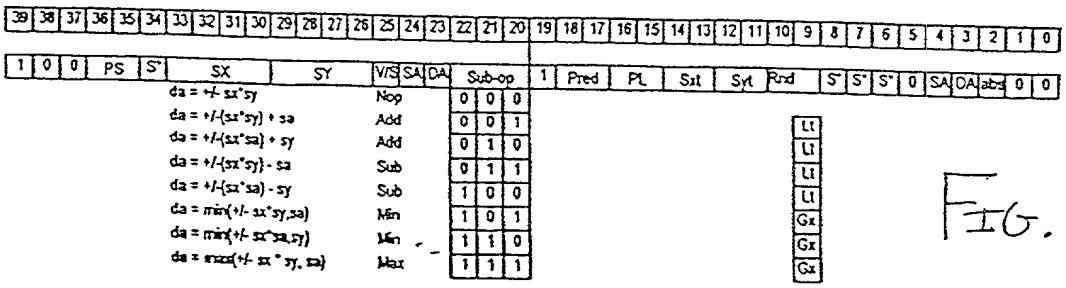


FIG. 6C

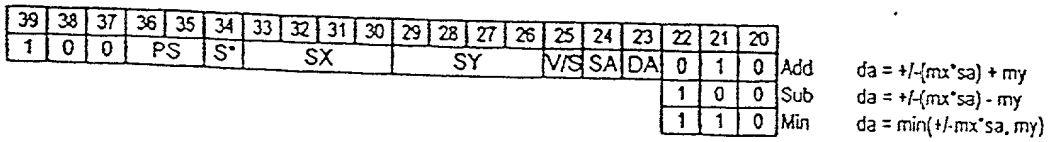
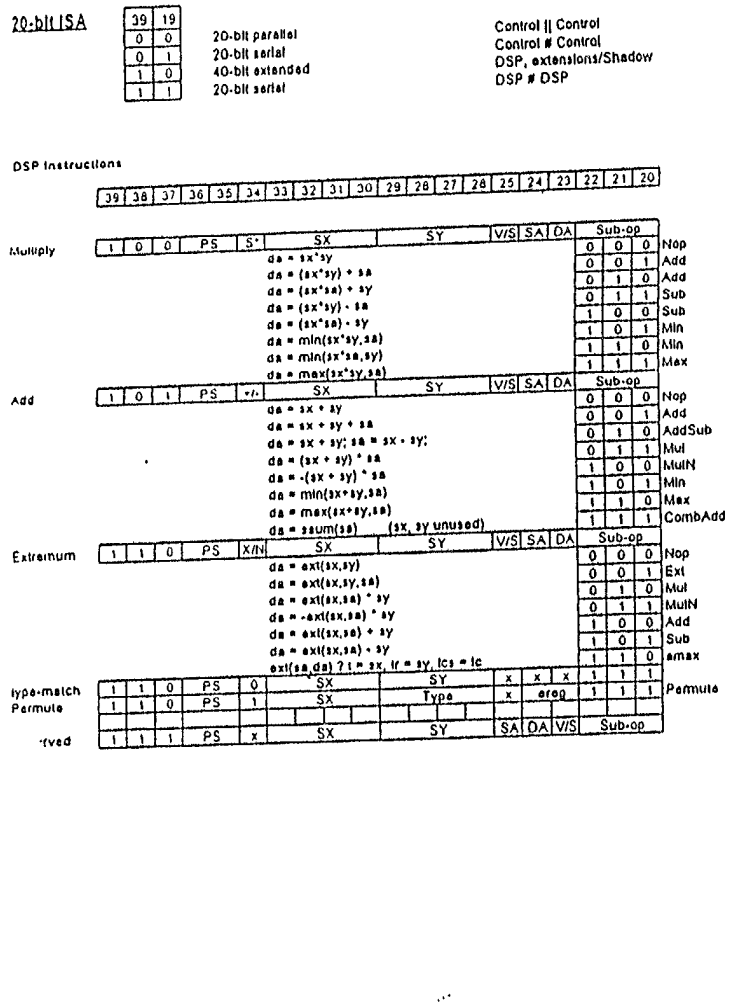


FIG. 6D


20-bit ISA
39 19
0 0 20-bit parallel
0 1 20-bit serial
1 0 40-bit extended
1 1 20-bit serial
Control || Control
Control # Control
DSP, extensions/Shadow
DSP # DSP
DSP Instructions
39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20
Multiply
Add
Extremum
Type-match Permute
Reserved
Sub-op
Nop
Add
AddSub
Mul
MulN
Min
Max
CombAdd
Ext
Sub
amax
Permute

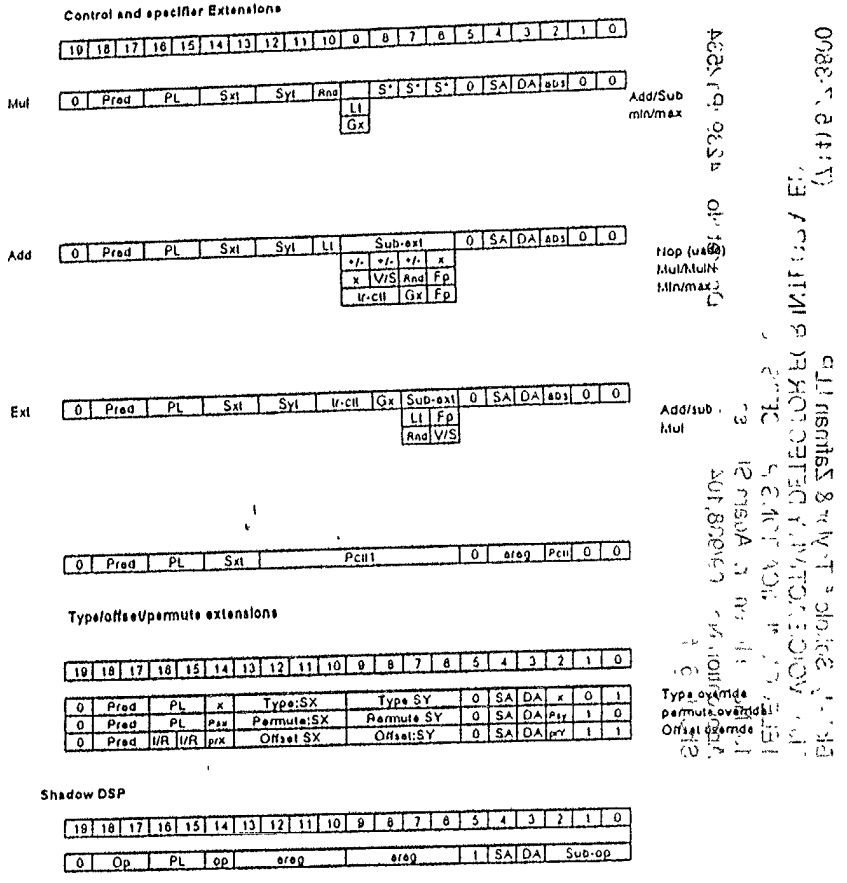

Control and specifier Extensions
Mul
Add
Ext
Add/Sub min/max
Nop (use Mul/MulN Min/max)
Add/sub Mul
Type/offset/permute extensions
Type override
permute override
Offset override
Shadow DSP

FIG. 6 E

Control Instructions

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
add,sub	L	Pred	0	0	0	RX					RY				RZ				+/-	0
max,min	L	Pred	0	0	0	RX					RY				RZ				X/N	1
Shift	L	Pred	0	0	1	RX					UI4				RZ				UI1	R/L
Logic	L	Pred	0	1	0	RX					RY				RZ				&, |	&|
Mux	L	Pred	0	1	1	RX					RY				RZ				Pd	0
mov	L	Pred	0	1	1	RX					DZ				Rxt	Dzt	0	0	0	1
addi	L	Pred	0	1	1	SI4					DZ				x	x	1	0	0	1
mov2erg	L	Pred	0	1	1	RX					unit		ereg		gd	type		1	0	1
Ldm	L	Pred	0	1	1	RX					DZ1				DZ2				1	1
tbits	L	Pred	1	0	0	UI4:POS					RZ				Rzt	UI4				0
btts	L	Pred	1	0	0	UI4:POS					RZ				Rzt	UI2		0	0	1
Setbit	L	Pred	1	0	0	UI4:POS					RZ				Rzt	UI1	UI1	1	0	1
Movl	L	Pred	1	0	0	SI8									RZ				-1	1
Jmp	L	Pred	1	0	1	SI9										0	Pred		0	0
Call	L	Pred	1	0	1	SI9										1	Pred		0	0
Loop	L	Pred	1	0	1	UI5 : Lcount					UI5: Lsize							UI2: Lsl	0	1
Jmpi	L	Pred	1	0	1	RX					x	x	x	x	x	0	Pred		1	0
Calli	L	Pred	1	0	1	RX					x	x	x	x	x	1	Pred		1	0
Loopi	L	Pred	1	0	1	RX					x	UI5: Lsize						UI2: Lsl	1	1
Tst	L	Pred	1	1	0	RX					RY				PZ				=, <, >	0
Testbit	L	Pred	1	1	0	RX					UI5					PZ			B	0	1
Andp, orp	L	Pred	1	1	0	Pa			Pb			Pc			PZ				&|	1	1
Load	L	Pred	1	1	1	MX					RZ				Ext				0	0	0
Store	L	Pred	1	1	1	MZ					RX				Ext				1	0	0
eLoad	L	Pred	1	1	1	MX					RZ				1	1	1	0	0	0	0
eStore	L	Pred	1	1	1	MZ					RX				1	1	1	1	0	0
Extended	L	Pred	1	1	1	Bits 27:16													1	0
Logic2	L	Pred	1	1	1	RX					RY/RZ				Rxt	Ryt	& , | , &| , !			0	1
mov-erg	L	Pred	1	1	1	unit		ereg			RZ				gd	Sft			0	1	1
Crb	L	Pred	1	1	1	RX					RZ				s/m	0	0	1	1	1
Parity	L	Pred	1	1	1	RX					PZ			O/E	0	1	0	1	1	1
Stm	L	Pred	1	1	1	MZ					RX				1	1	0	1	1	1
Abs	L	Pred	1	1	1	RX					RZ				0	0	1	1	1	1
Neg	L	Pred	1	1	1	RX					RZ				0	1	1	1	1	1
Div-step	L	Pred	1	1	1	RX					RZ				1	0	1	1	1	1
& Set	L	Pred	1	1	1	RX					PZ			0	1	1	1	1	1	1
[illegible]	[illegible]																			
Return	L	Pred	1	1	1	Pred		I-ctl			0	1	0	1	1	1	1	1	1	1
Zero-ac	L	Pred	1	1	1	ac #					1	1	0	1	1	1	1	1	1	1
eSync	L	Pred	1	1	1	RZ					0	1	1	1	1	1	1	1	1	1
Swi	L	Pred	1	1	1	UI3				0	1	1	1	1	1	1	1	1	1	1
Nop	L	Pred	1	1	1	UI3				1	1	1	1	1	1	1	1	1	1	1

<Bit1, Bits9-6> == UI5 (Shift Amount)

<Bit3, Bits13-10> == UI5 :POS

FIG. 6F

Extended Control

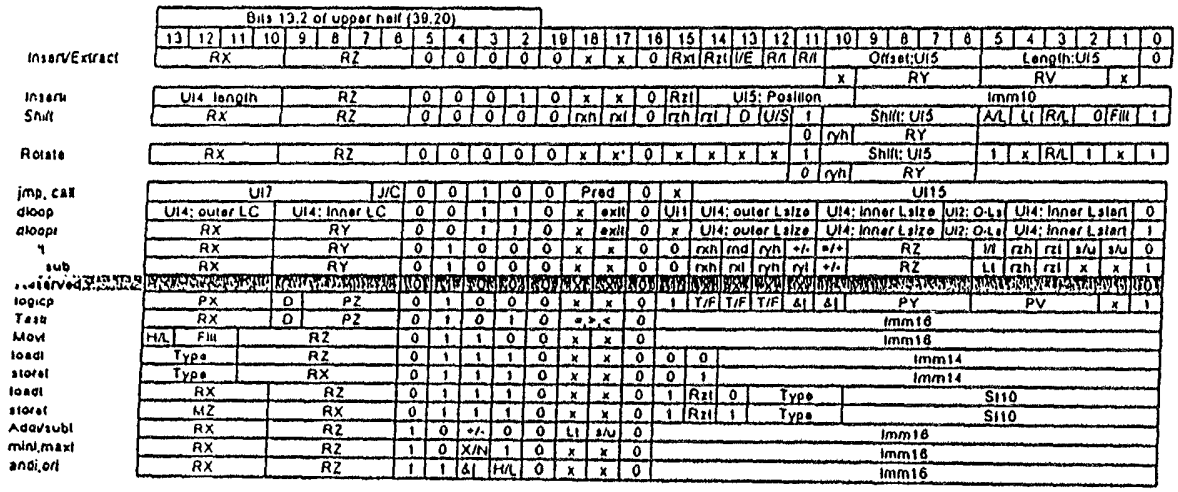


FIG. 6 G

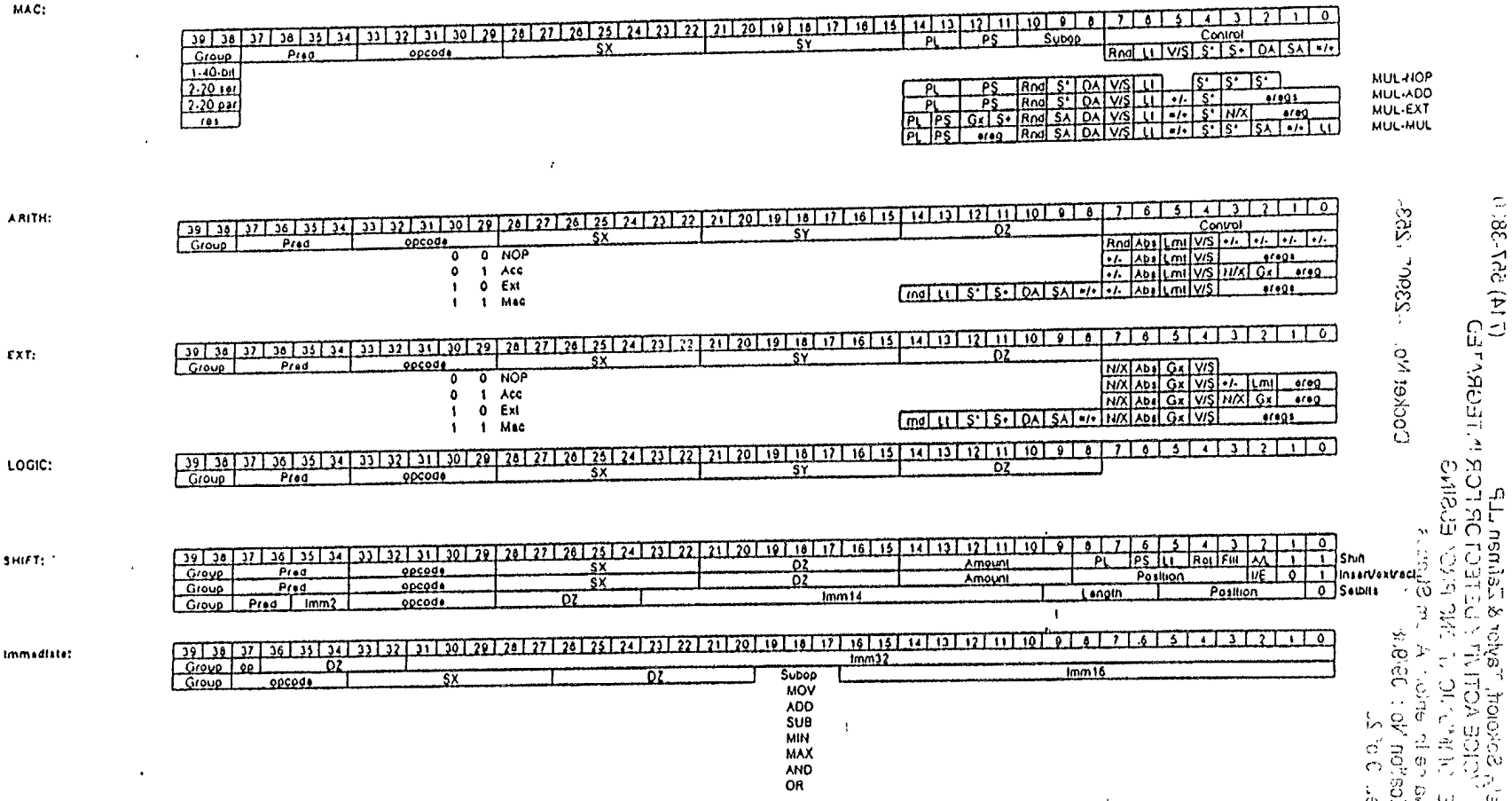

MAC:
ARITH:
EXT:
LOGIC:
SHIFT:
Immediate:
Test:
Branch:
Misc:
MUL-NOP
MUL-ADD
MUL-EXT
MUL-MUL
NOP
Acc
Ext
Mac
Shift
Insert/extract
Subbits
Subop
MOV
ADD
SUB
MIN
MAX
AND
OR

FIG. 6H

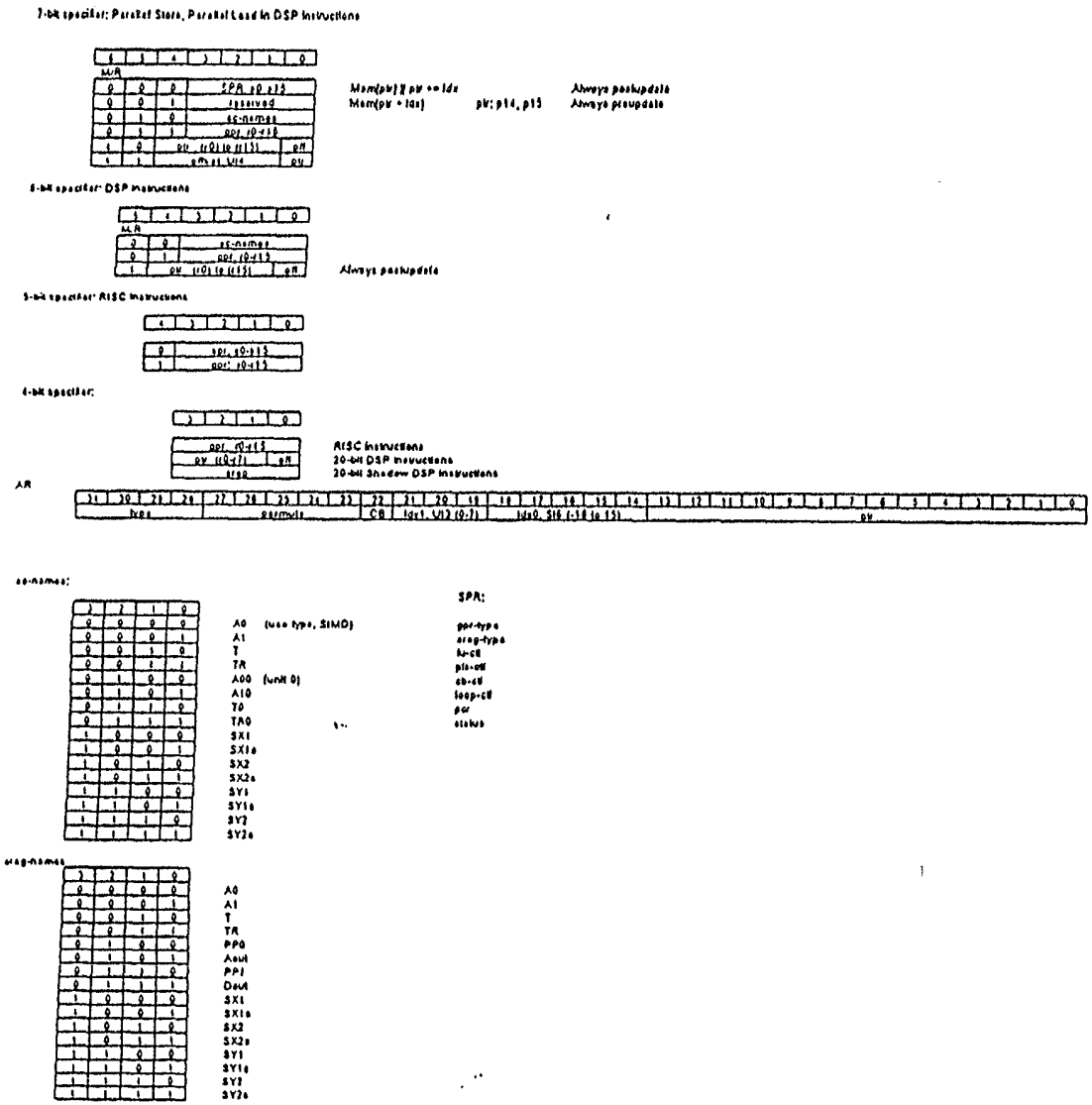


FIG. 6I

FIG. 7

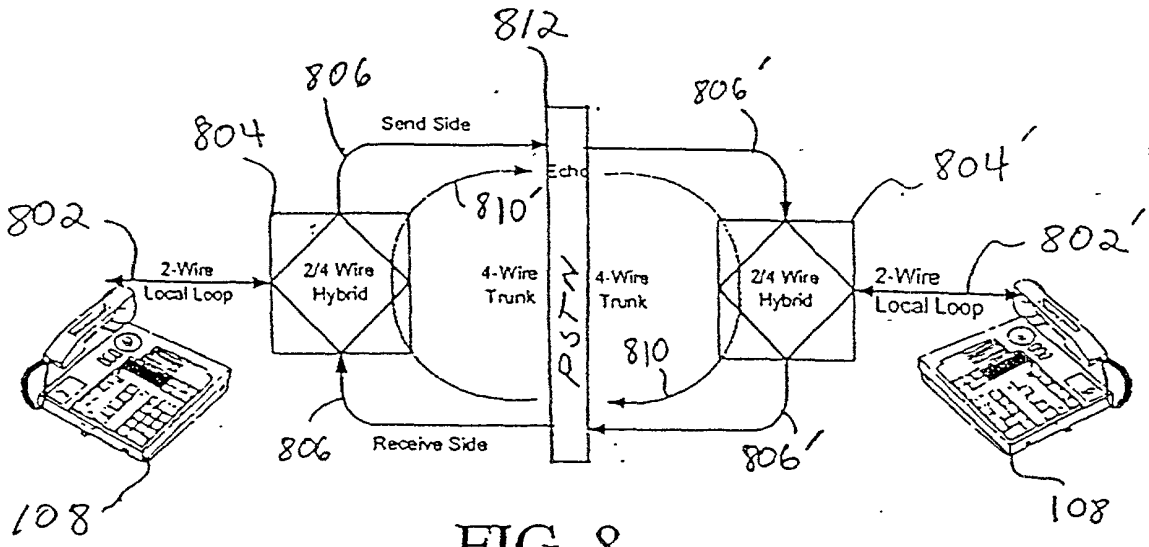


FIG. 8
(PRIOR ART)

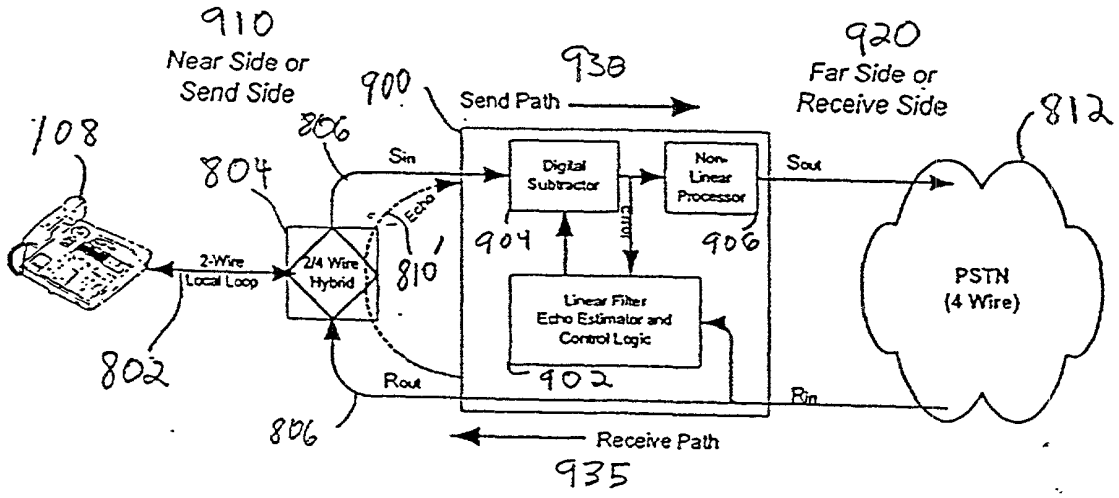


FIG. 9
(PRIOR ART)

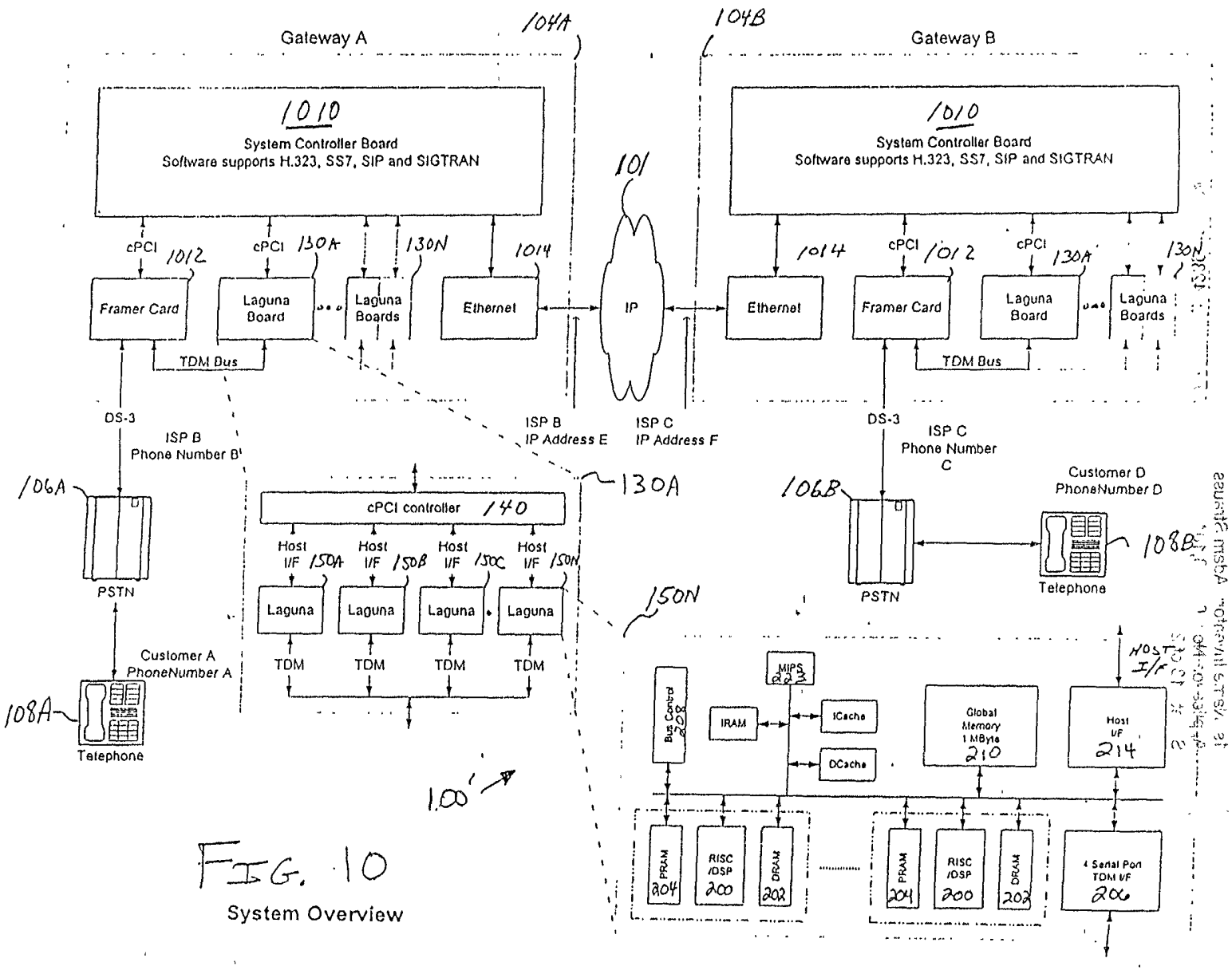


FIG. 10
System Overview

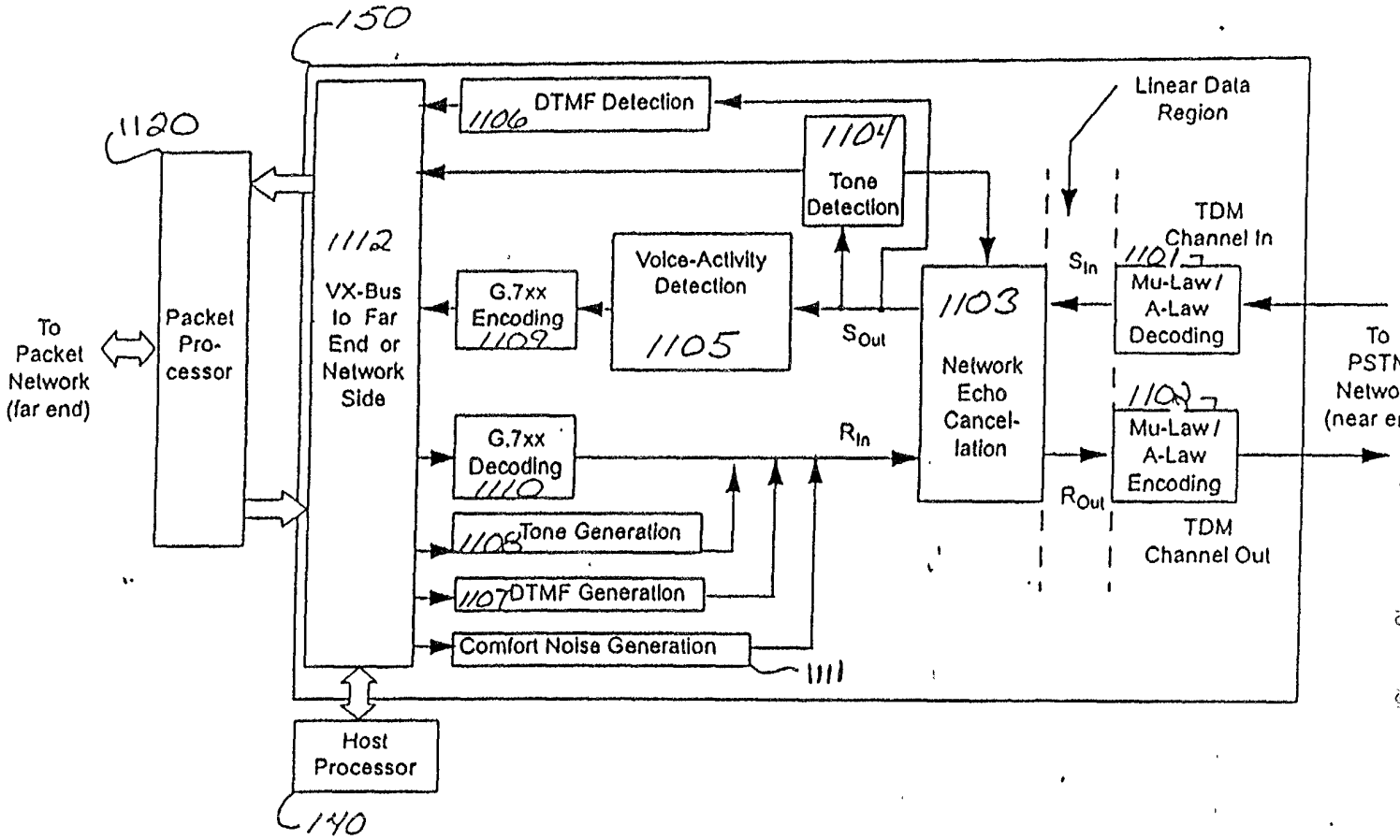


FIG. 11

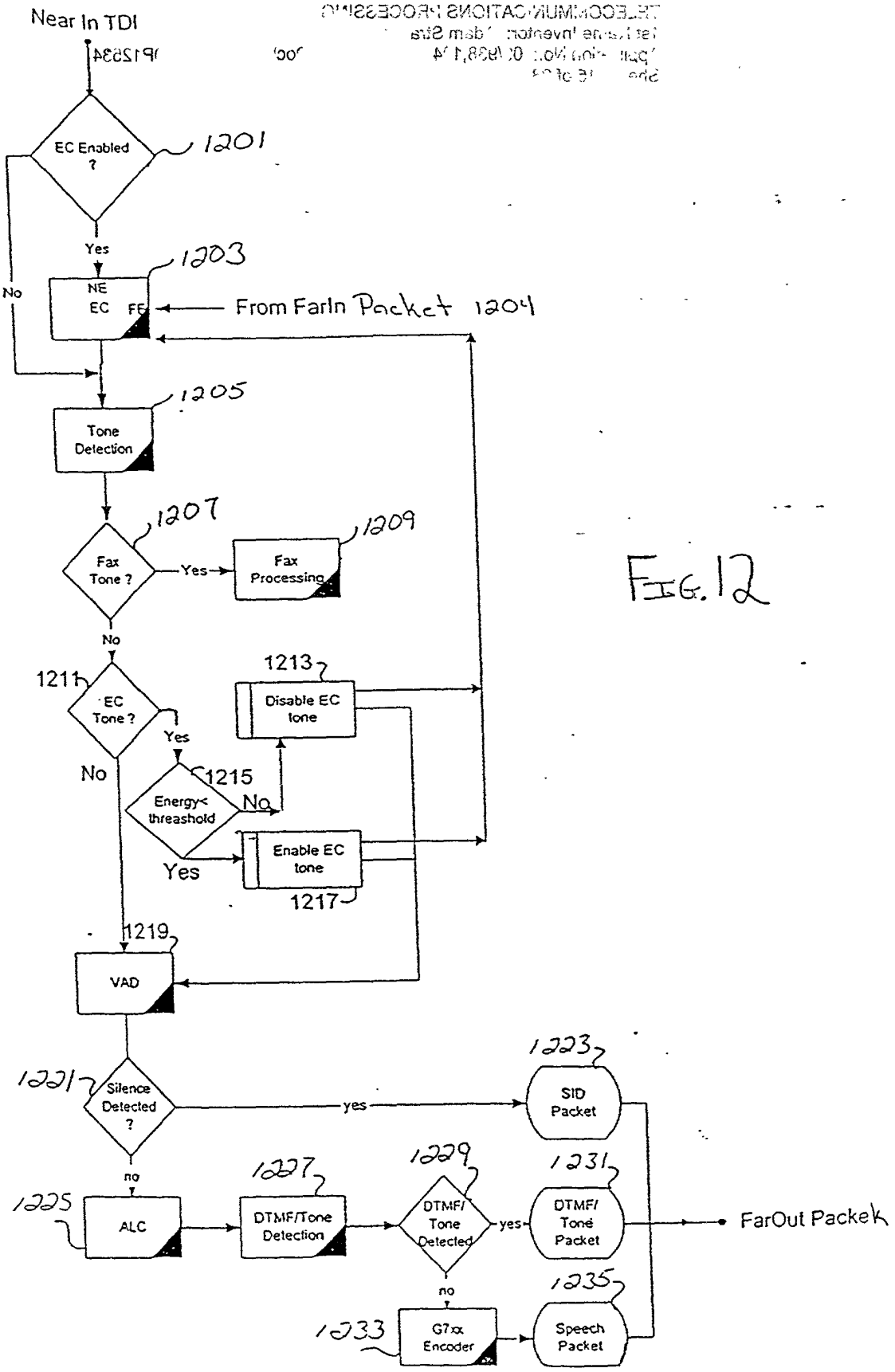

Near In TDI
EC Enabled ?
1201
Yes
No
1203
NE EC FE
From FarIn Packet 1204
1205
Tone Detection
1207
Fax Tone ?
Yes
1209
Fax Processing
No
1211
EC Tone ?
Yes
No
1213
Disable EC tone
1215
Energy< threashold
No
Yes
Enable EC tone
1217
1219
VAD
1221
Silence Detected ?
yes
1223
SID Packet
no
1225
ALC
1227
DTMF/Tone Detection
1229
DTMF/ Tone Detected
yes
1231
DTMF/ Tone Packet
FarOut Packek
no
1233
G7xx Encoder
1235
Speech Packet

FIG. 12

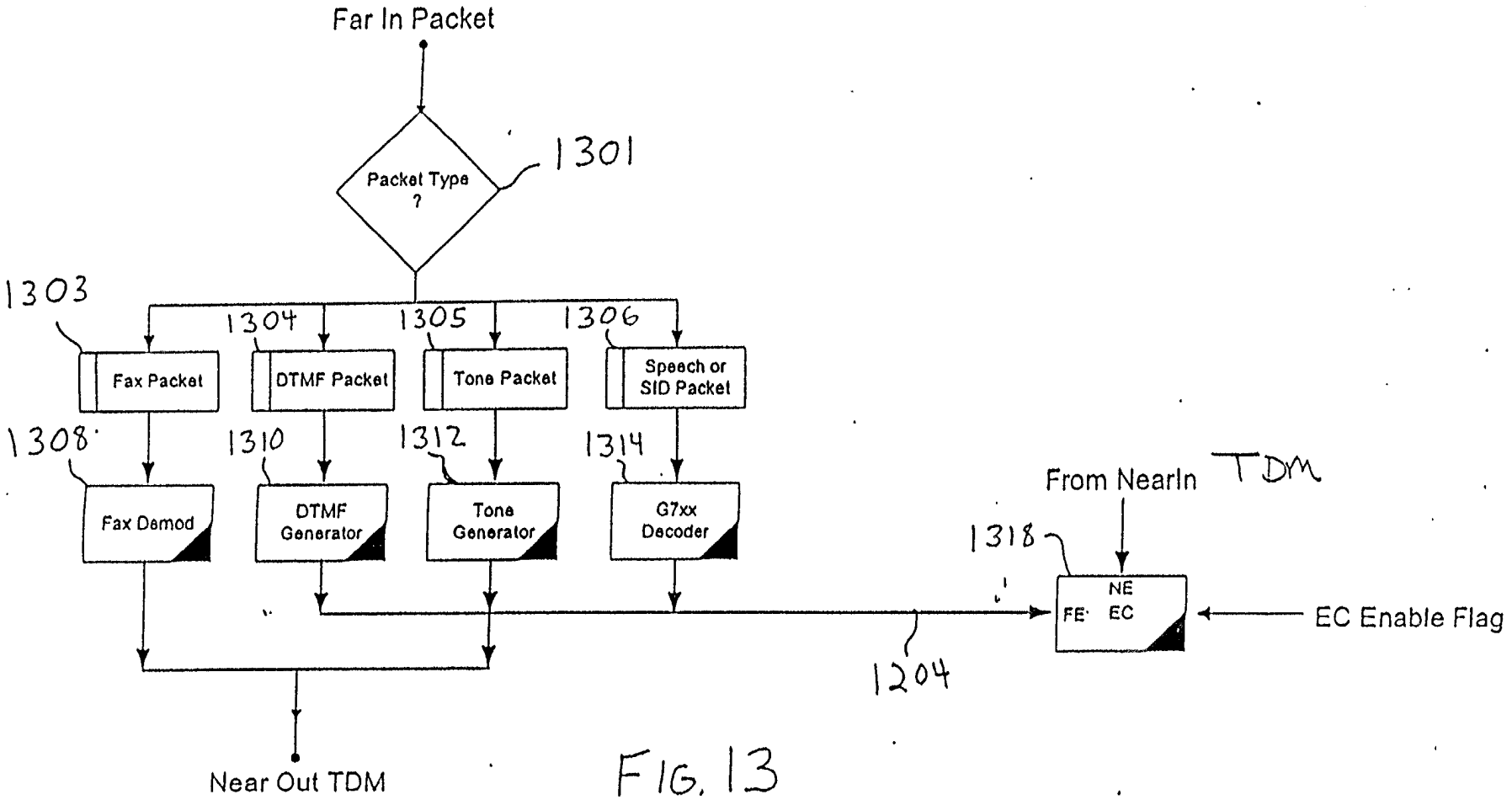


FIG. 13

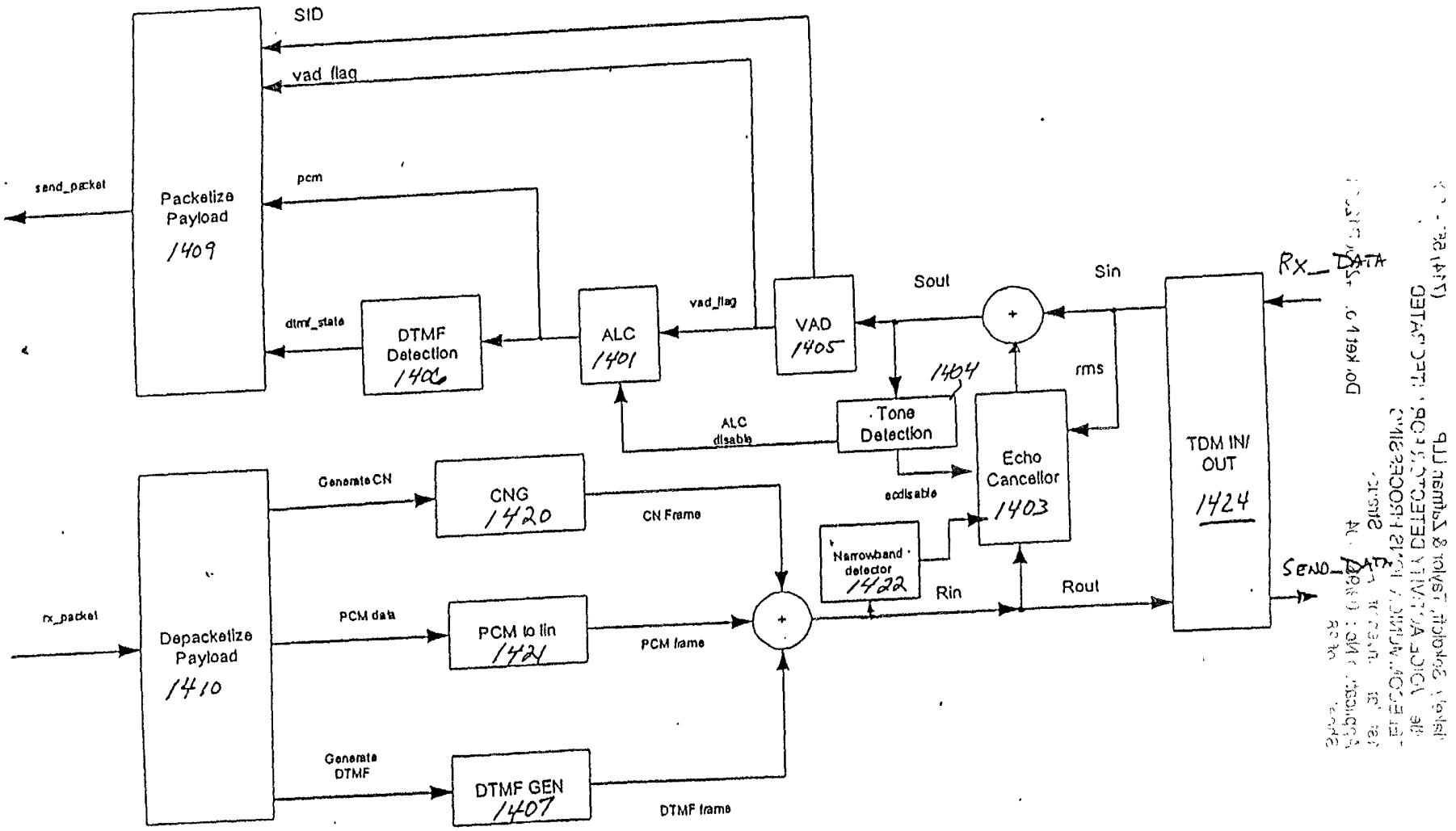


FIG. 14A

VxTel Voice Activity Detection Algorithm

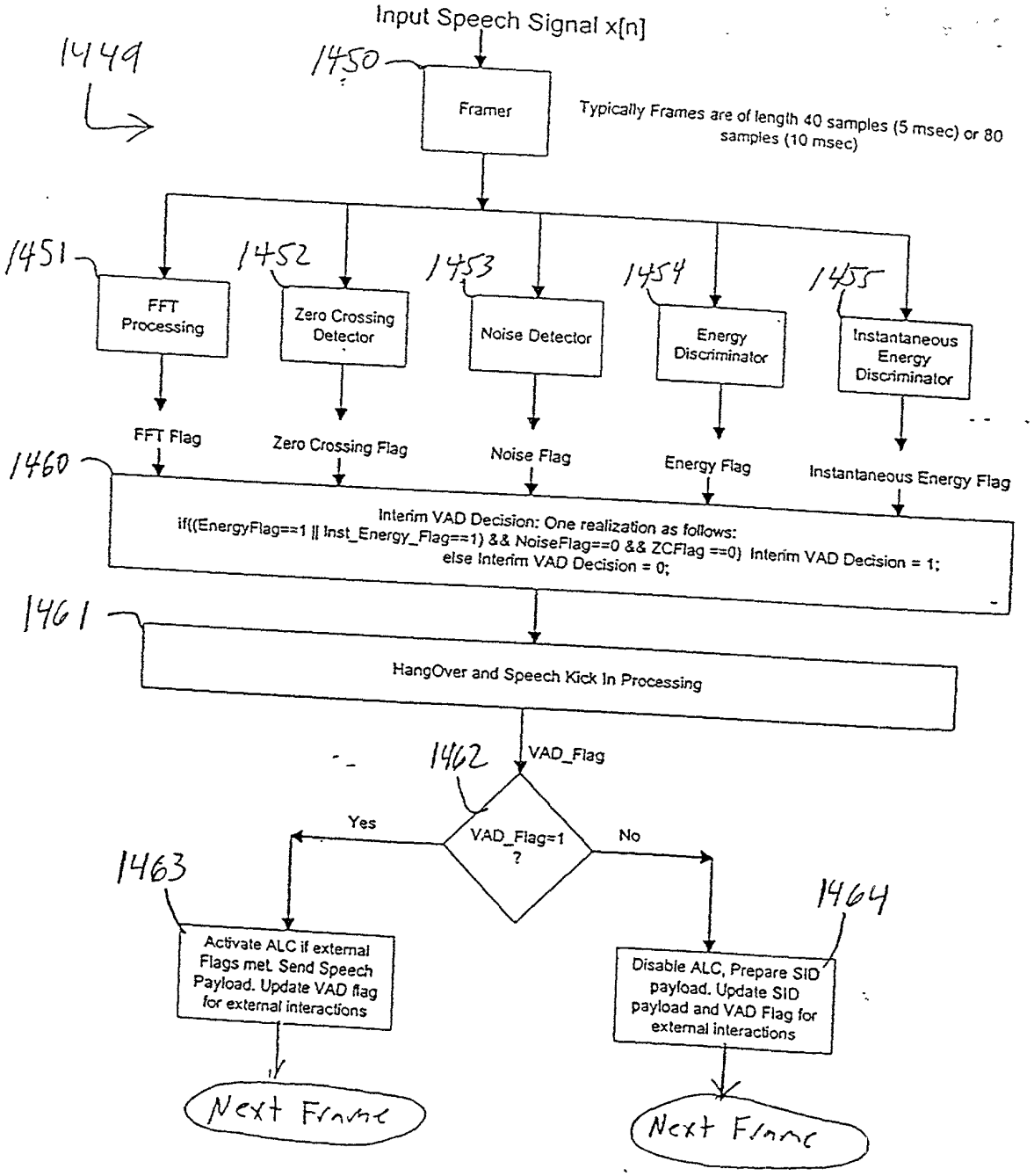


FIG. 14B

FFT Processing of Input Speech for VAD 1451

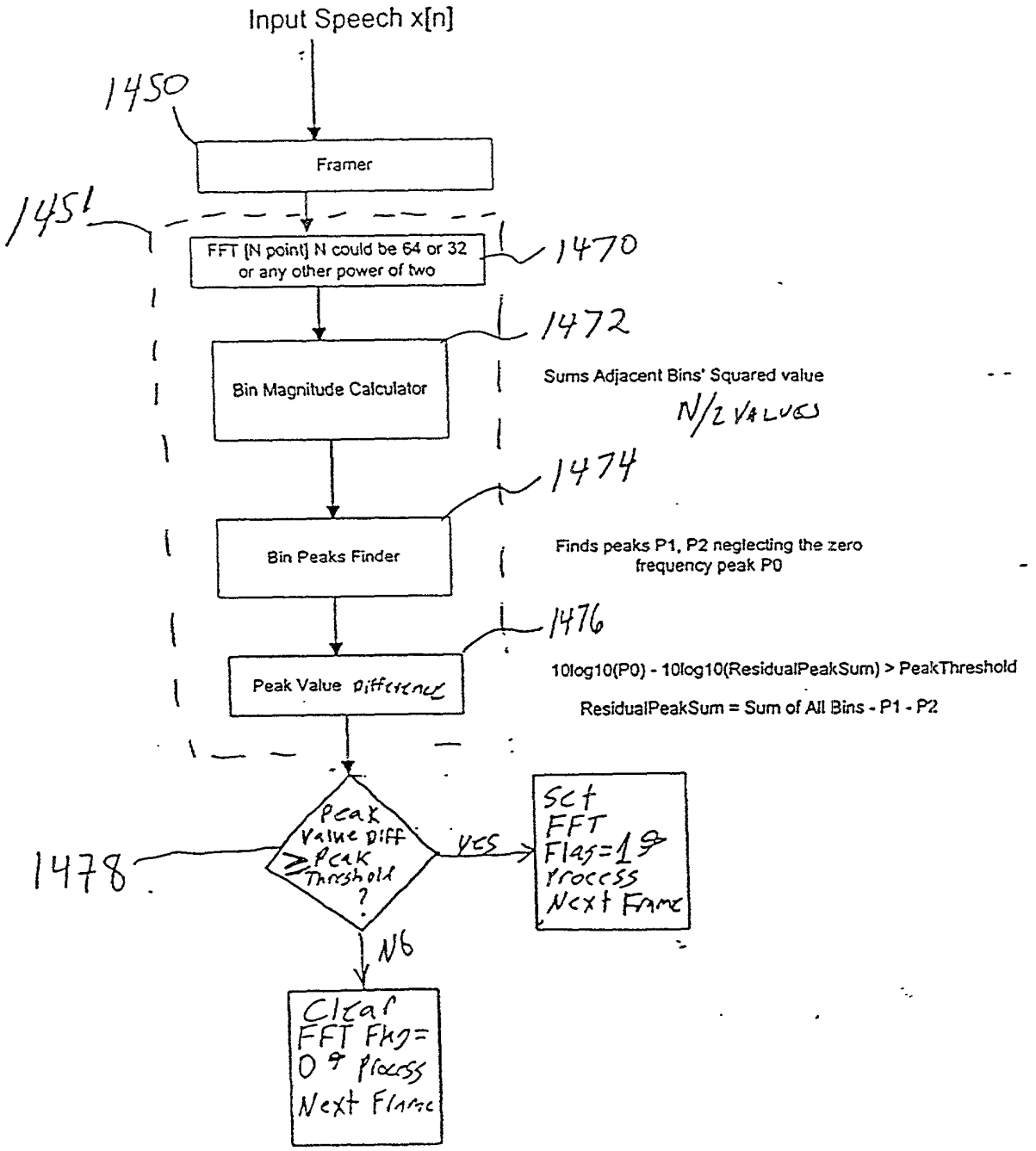


FIG. 14C

Zero Crossing Detector 1452

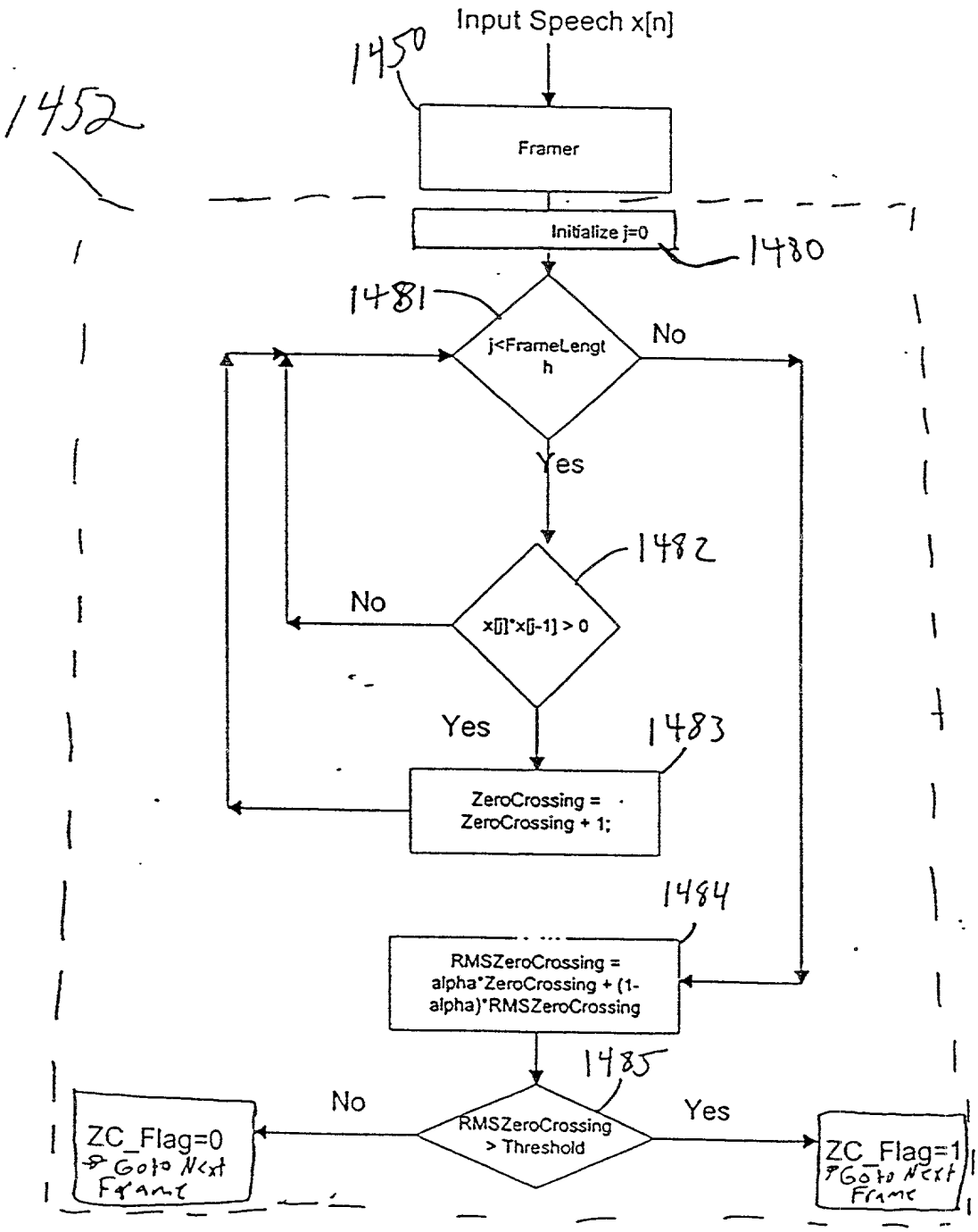


FIG. 14D

Noise Detection in VAD

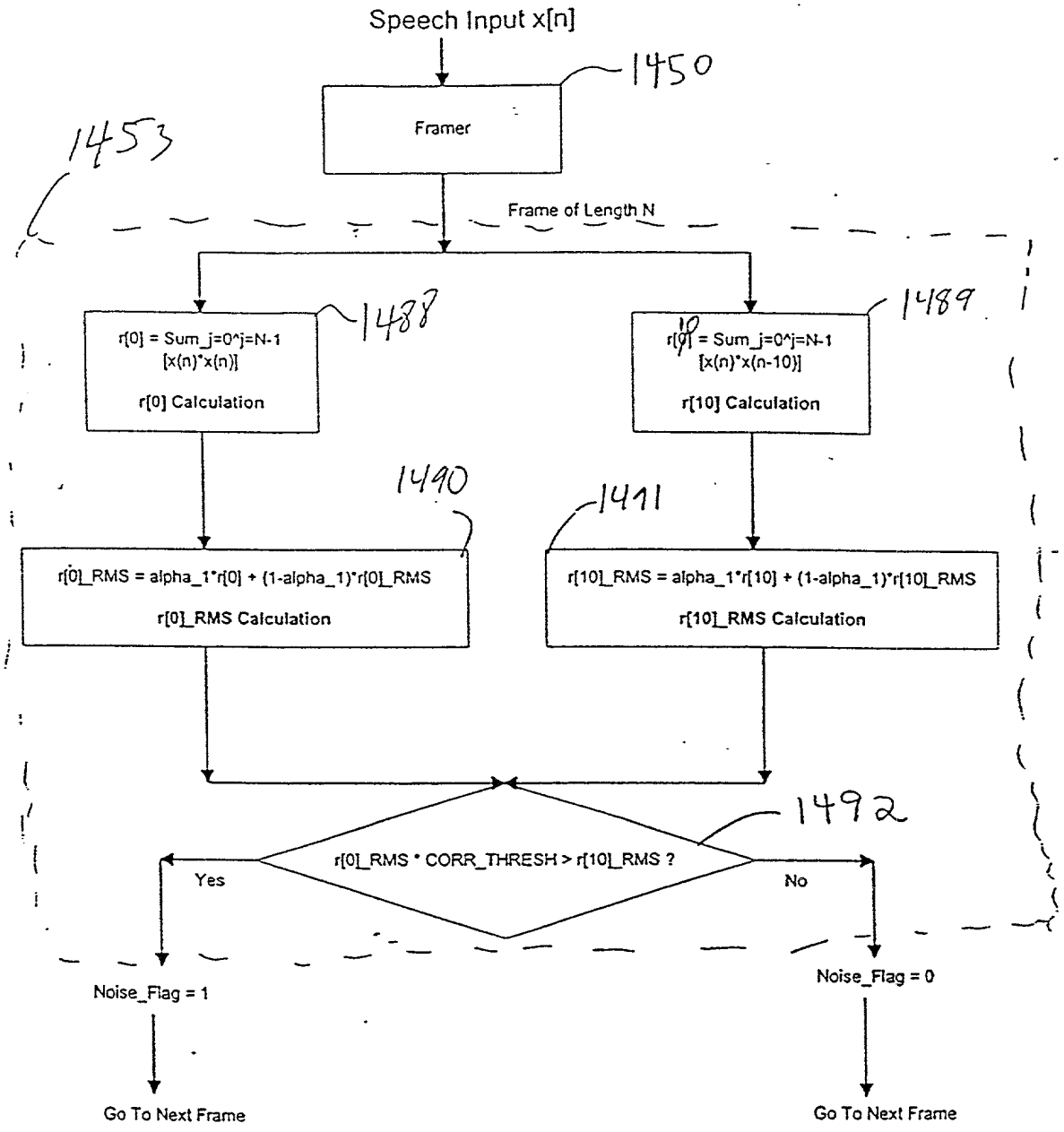


FIG. 14E

Energy Discriminator 1454

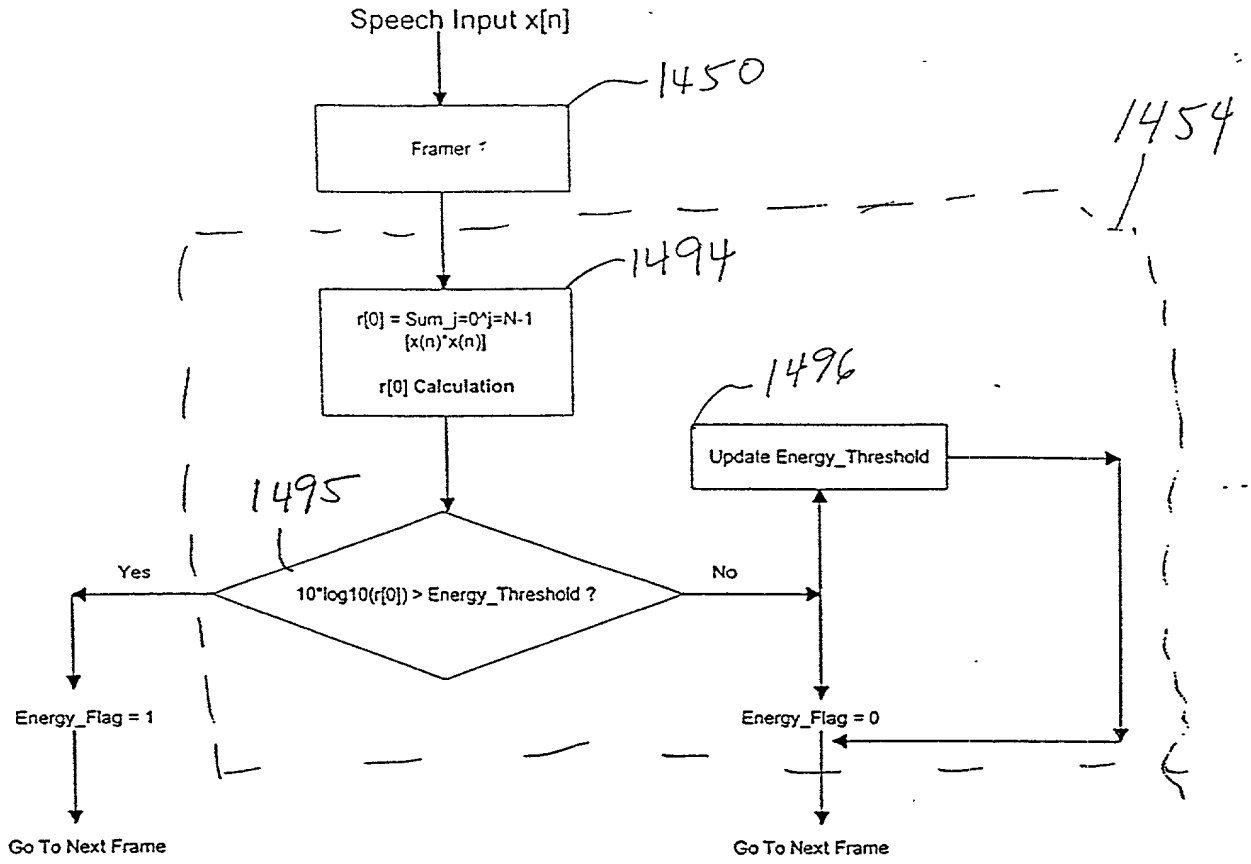


FIG. 14F

Instantaneous Energy Discriminator 1455

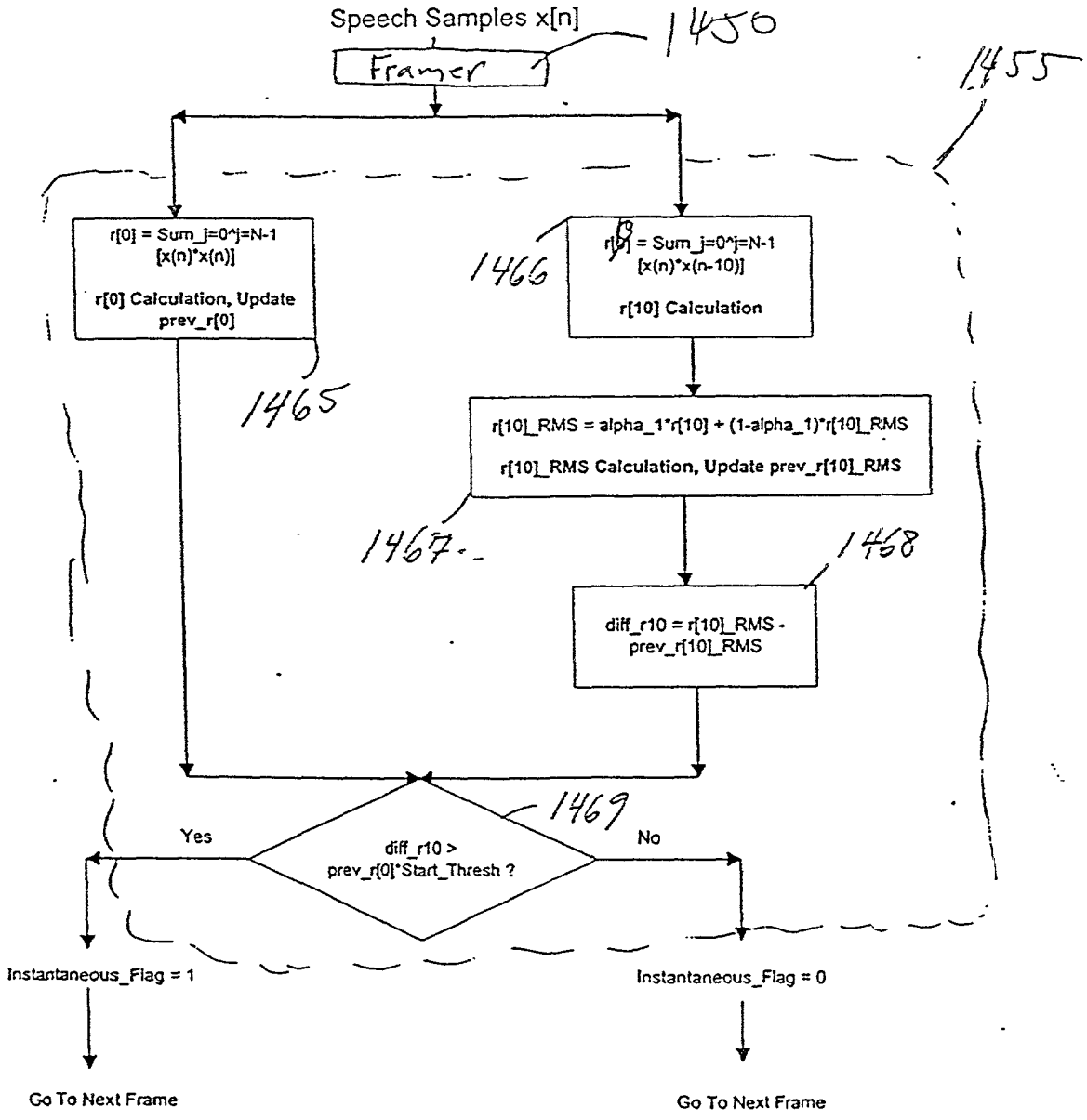


Fig. 14G

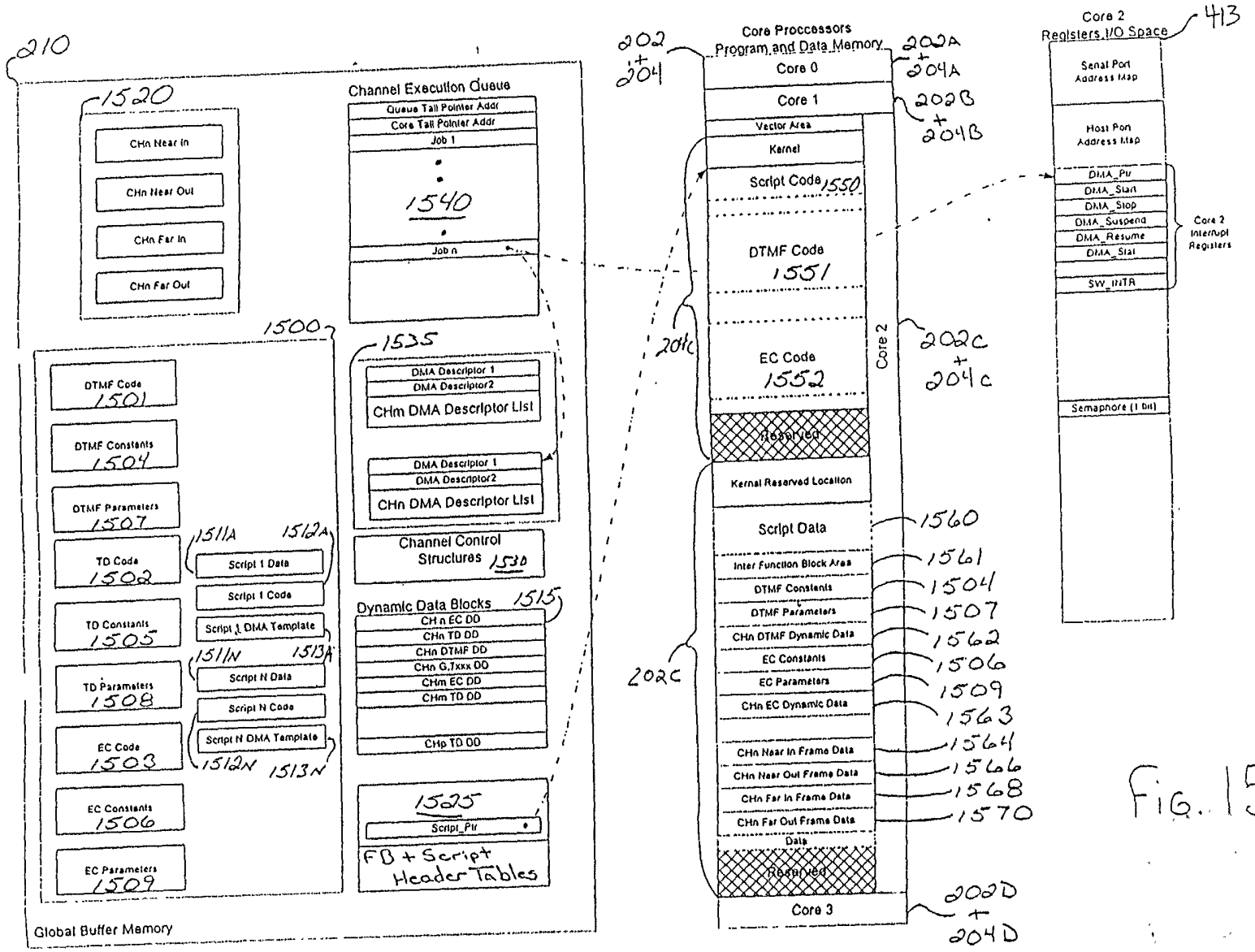

210
1520
CHn Near In
CHn Near Out
CHn Far In
CHn Far Out
Channel Execution Queue
Queue Tail Pointer Addr
Core Tail Pointer Addr
Job 1
1540
Job n
1500
1535
DMA Descriptor 1
DMA Descriptor2
CHm DMA Descriptor List
DMA Descriptor 1
DMA Descriptor2
CHn DMA Descriptor List
DTMF Code 1501
DTMF Constants 1504
DTMF Parameters 1507
TD Code 1502
TD Constants 1505
TD Parameters 1508
EC Code 1503
EC Constants 1506
EC Parameters 1509
1511A
1512A
Script 1 Data
Script 1 Code
Script 1 DMA Template
1513A
1511N
Script N Data
Script N Code
Script N DMA Template
1512N
1513N
Channel Control Structures 1530
Dynamic Data Blocks 1515
CH n EC DD
CHn TD DD
CHn DTMF DD
CHn G.7xxx DD
CHm EC DD
CHm TD DD
CHp TD DD
1525
Script_Ptr
FB + Script Header Tables
Global Buffer Memory
202 + 204
Core Proccessors Program and Data Memory
202A + 204A
Core 0
202B + 204B
Core 1
Vector Area
Kernel
Script Code 1550
DTMF Code 1551
201c
EC Code 1552
202C + 204c
Core 2
Reserved
Kernal Reserved Location
Script Data
1560
Inter Function Block Area
1561
DTMF Constants
1504
DTMF Parameters
1507
CHn DTMF Dynamic Data
1562
EC Constants
1506
EC Parameters
1509
CHn EC Dynamic Data
1563
CHn Near In Frame Data
1564
CHn Near Out Frame Data
1566
CHn Far In Frame Data
1568
CHn Far Out Frame Data
1570
Data
Reserved
202C
202D + 204D
Core 3
Core 2 Registers I/O Space
413
Serial Port Address Map
Host Port Address Map
DMA_Ptr
DMA_Start
DMA_Stop
DMA_Suspend
DMA_Resume
DMA_Stat
SW_INTR
Core 2 Interrupt Registers
Semaphore (1 bit)

Fig. 15

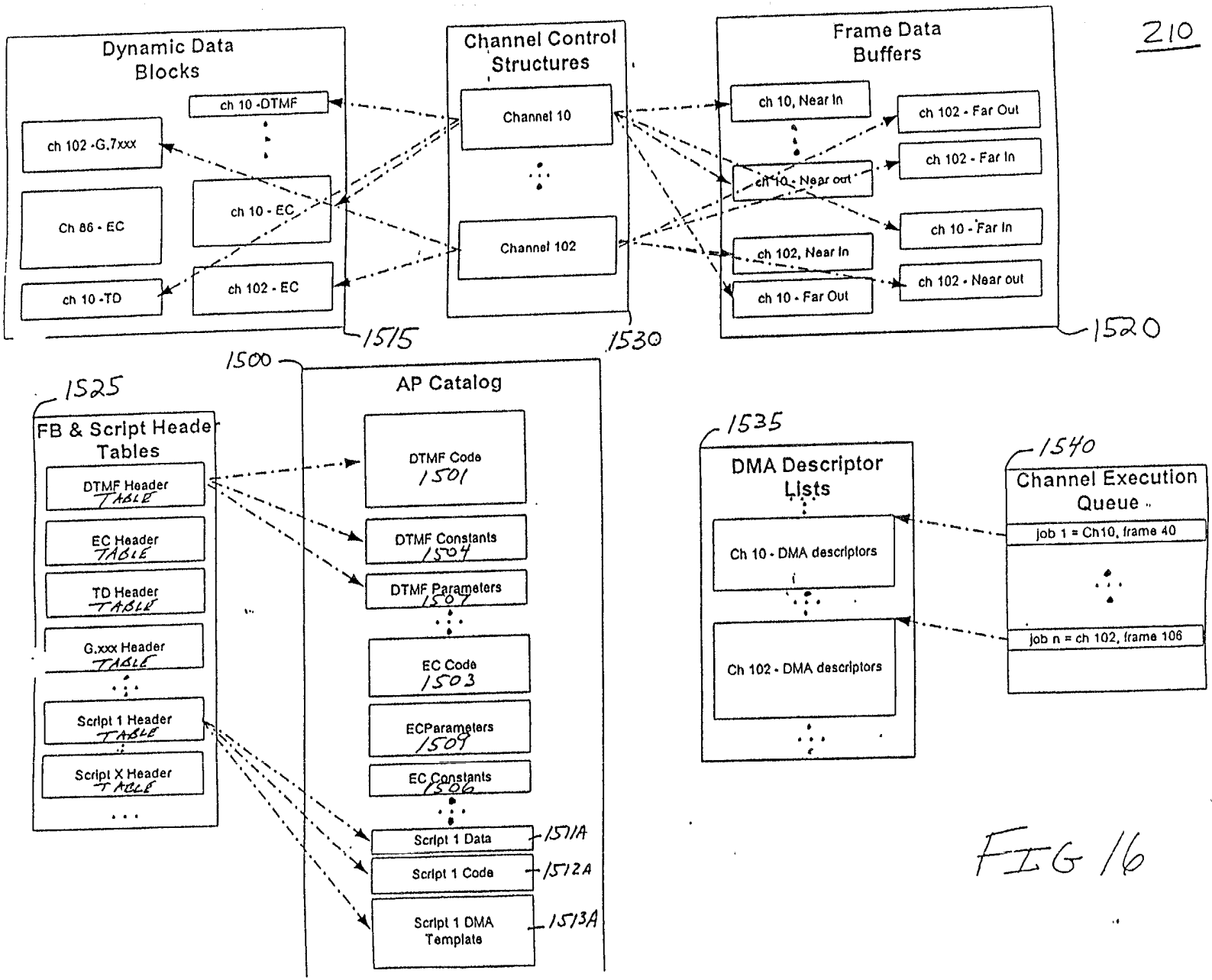


FIG 16

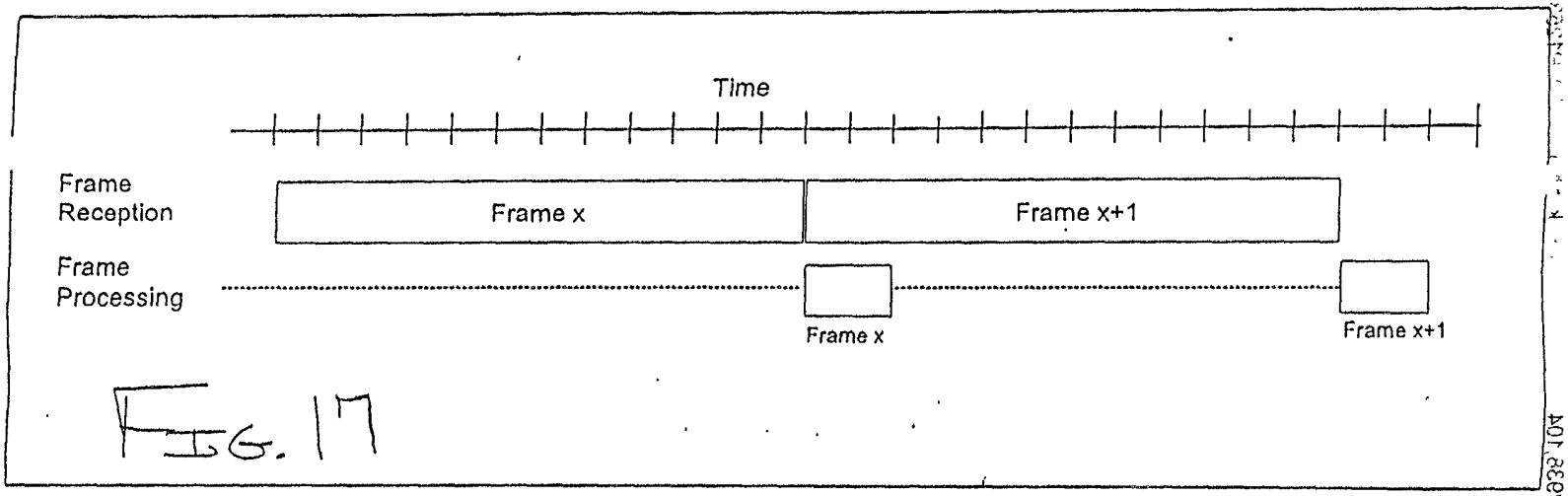

Time
Frame Reception
Frame x
Frame x+1
Frame Processing
Frame x
Frame x+1

Fig. 17

FIG. 18